Amendments to the Claims

The following listing of claims will replace the original listing of claims.

Listing of Claims

1. (Amended) A method for making a semiconductor device having a p-type device region, comprising the steps of:

(i) forming an initial region to an initial depth from at least a portion of an initial surface of a semiconductor substrate which has a conductivity type and an original bulk spreading resistivity,

(ii) heating said initial region, therein to develop an initial spreading resistivity profile having a peak, with peak value greater than said bulk spreading resistivity,

(iii) removing material from said initial surface portion, thereby forming said p-type device region having a new surface from which said resistivity peak is at a reduced depth.

2. (Unchanged) The method of claim 1, wherein step (i) comprises implanting particles.

3. (Unchanged) The method of claim 2, wherein said particles are selected from the group consisting of neutrons, protons, hydrogen ions, inert-gas ions and metallic ions.

4. (Unchanged) The method of claim 1, wherein said substrate has p-type conductivity.

5. (Unchanged) The method of claim 1, wherein said substrate has n-type conductivity and wherein, in step (ii), heating results in a change of conductivity to p type in said initial region.

6. (Unchanged) The method of claim 5, wherein heating for changing said conductivity type is distinct from heating to develop said initial spreading resistivity profile.

7. (Unchanged) The method of claim 1, wherein step (iii) comprises at least one of plasma etching, chemical etching and chemical-mechanical polishing.

8. (Unchanged) The method of claim 1, further comprising a step of selectively implanting dopant ions in said device region for forming channels for charge carriers.

9. (Unchanged) The method of claim 1, further comprising a step of selectively implanting dopant ions in said device region for forming source and drain regions.

10. (Amended) The method of claim 1, further comprising forming a CMOS structure in said p-type device region.

11. (Amended) The method of claim 10, wherein forming said CMOS structure comprises forming a trench between NMOS and PMOS devices, to a depth of at least to said depth of said peak of said spreading resistivity of said p-type device region.

12. (Amended) The method of claim 1, further comprising a step of epitaxially growing a crystalline region on said p-type device region.

13. (New) The method of claim 1, wherein heating of said initial region is to a temperature of approximately at least 900 degrees C.